WHAT IS CLAIMED IS:

1. A system for performing clock and data recovery on an incoming serial data stream comprising means for oversampling the incoming stream including;

a) a detector for digitally locating the edge location of a bit in a data stream;

b) a generator for creating an early and a late signal if the detected edge is not in its expected location and for sending the signal to a phase rotator control state machine,

c) the phase rotator control state machine serving to process the early or late outputs from the edge location detector, and

d) a phase rotator having phase settings that are controlled by the phase rotator control state machine.

2. The system according to claim 1 wherein the edge location detector is provided with means for detecting at least three evenly spaced samples of each bit.

3. The system according to claim 2 further including a sample processing algorithm for centering the bit edge in the middle between two samples.

4. The system according to claim 3 wherein the sample processing algorithm comprises an adaptive behavior algorithm.

5. The system according to claim 1 wherein the phase rotator is a 54 step rotator comprising six phases with three inter-slice phase steps further divided by three.

6. The system according to claim 1 further including a phase locked loop comprising a digital coarse loop and an analog fine loop, wherein the digital coarse loop provides a PLL frequency control signal to the analog fine loop.

7. The system according to claim 7 wherein the phase locked loop controls a three-stage ring oscillator running at one-half bit frequency.

8. The system according to claim 1 wherein the phase rotator controls the phase output of a clock generator.

9. The method for improving the bit error rate performance during clock and data recovery on an incoming serial data stream comprising oversampling the incoming stream including the steps of:

a) digitally detecting the edge location of a bit in a data stream;

b) generating an early or a late signal if the detected edge is not in its expected location;

c) sending the early or late signal to a phase rotation control state machine,

d) processing the early or late outputs from the edge location detector using the phase rotation control state machine; and

e) controlling the phase rotation using phase settings that are determined by the phase rotation control state machine.

10. The method according to claim 9 wherein at least three evenly spaced samples are obtained for each bit.

11. The method according to claim 10 wherein a sample processing algorithm centers the bit edge in the middle between two of the samples.

12. The method according to claim 11 wherein the sample processing algorithm is an adaptive behavior processing algorithm.

13. The method according to claim 9 wherein a feed back loop suppresses low frequency jitter and a feed forward loop suppresses high frequency jitter.

14. The method according to claim 9 wherein the phase rotation is used to control the phase output of a clock generator.

15. The method according to claim 9 wherein the samples are positioned so that none are on the bit edge, and are placed on either side of the bit edge.

16. The method according to claim 9 wherein the phase locked loop is used to control a three-stage ring oscillator running at one-half bit frequency.

17. A receiver core for performing clock and data recovery on a wire transmitted incoming serial data stream, comprising :

a) a phase locked loop running at one-half of the bit frequency;

b) a ring oscillator controlled by a voltage signal and a current signal from the phase locked loop;.

c) a 54 step phase rotation device under the control of a phase rotator control state machine to control phase output of a clock generator;

d) a detector for digitally detecting the edge position in a data stream;

e) means for digitally selecting the optimum data sample;

f) a generator for generating an early and a late signal if the detected edge is not in its expected position and for sending the signal to a phase rotation control state machine; and

g) a phase rotator control state machine to process the early or late outputs from the edge correlation outputs to control the phase settings of the phase rotator, wherein the early and late signal generating circuitry controls the output phase position of a phase locked loop, said phase locked loop includes a feed back loop to suppress low frequency jitter and a feed forward loop to suppress high frequency jitter.